The Effect of Phosphorus Incorporation into SiO_2/4H-SiC (0001) Interface on Electro-Physical Properties of MOS structure

K. Król [1,2], P. Konarski [2], M. Miśnik [2], M. Sochacki [1] and J. Szmidt [1]

[1] *Institute of Micro- and Optoelectronics Warsaw University of Technology, Koszykowa 75, 00-662 Warsaw, Poland*
[2] *Tele- and Radio Research Institute, Ratuszowa 11, 03-450 Warsaw, Poland*

Charge trapping properties of silicon dioxide as a gate dielectric in silicon-carbide (SiC) MOS structure have been extensively studied for last decade. Although the obtained experimental results allowed to create the empirical description of the main trap properties as the trap density distribution in the band gap of SiC [1] and many of the detected traps were assigned to the physical defects based on density functional theory (DFT) calculation, the origin of the trap states localized near the conduction band edge of SiC still remains unclear. Beyond the theoretical considerations the experimental studies of trapped charge associated with nitrogen and phosphorus incorporation were performed [2]. The phosphorus incorporation is considered to be the most suitable for trap density reduction, despite the physical aspects of the process, are still poorly understood. In this work, phosphorus influence on the near interface traps (NIT) was investigated. The near interface traps are associated with structural defects localized in the dielectric layer close enough to the interface region to exchange charge with semiconductor due to tunneling mechanism. These trap states determine MOS structure properties and have not been investigated yet.

The main aim of this work is the investigation of phosphorus incorporation into thermal SiO_2/4H-SiC system interface and the influence of the process on the NIT trap properties and long-term stability of this structure. Two methods were applied to supply phosphorus: ion implantation and $POCl_3$ annealing. The electrical response of NITs was investigated based on Fleetwood's method [3], developed and described by Gutt [4]. Secondary Ion Mass Spectrometry (SIMS) was used to find correlation between the observed electrical properties and chemical composition. In particular, phosphorus concentration and its spatial distribution in the dielectric layer are investigated. The relations between NITs generation and phosphorus concentration and/or its distribution are proposed.

The obtained results show presence of a new type NIT trap. Regardless of technology used, the signal from the new type trap was strongly correlated with the phosphorus concentration near the SiO_2/SiC interface. The basic properties of the trap centers were examined and measured.

Both methods of P incorporation result in a significant reduction of fast responding trap states and both can reduce amount of the charge trapped in NITs, efficiently improving the long-term reliability of the MOS devices.

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[1] V. Afanasev, M. Bassler, G. Pensl i M. Schulz, *Phys. Stat. Sol. (A),* **162**, 321 (1997).
[2] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, T. Fuyuki, *IEEE Electron. Dev. Lett.,* **31**, 710 (2010).
[3] D. M. Fleetwood, N. S. Saks, *J. Appl. Phys.*, **79,** 1583 (1996)
[4] Gutt T, *Proc. of the 33rd International Convention MIPRO 2010*, **1**, 48, (2010)