Electrical Characterization of ZnO-based Junctions Prepared by the Atomic Layer Deposition Method – Possible Ways to Improve the Device Rectifying Properties

Tomasz A. Krajewski[1], Ramón Schifano[1], Dmytro Snigurenko[1], Elżbieta Guziewicz[1], Krzysztof Kopalko[1], Marek Godlewski[1, 2], Krzysztof Gościński[1]

[1] *Institute of Physics, Polish Acad. of Sciences, Al. Lotników 32/46, 02-668 Warsaw, Poland*
[2] *Dept. of Mathematics and Natural Sciences College of Science*
Cardinal S. Wyszyński University, ul. Dewajtis 5, 01-815 Warsaw, Poland

ZnO is a promising material for a wide variety of device applications ranging from optoelectronic to piezoelectric and spintronic devices. One of the growth methods that gathers a rapidly increasing interest in this field is the Atomic Layer Deposition (ALD). Nowadays the ALD-ZnO films are tested as a promising candidate for transparent conductive electrodes in solar cells, parts of thin film transistors as well as selecting elements in the 3D memories based on a cross-bar architecture. For some of these devices a good quality rectifying junction is an essential element. In order to construct a ZnO-based diode with desired I-V characteristics the zinc oxide layer should reveal both low carrier concentration (responsible for the low reverse current) and their high mobility (for a high driving current of the junction). These two features can be achieved by proper adjustment of the ZnO growth conditions [1].

As we have already demonstrated, the ALD-ZnO films 100 nm to 400 nm thick deposited between 100 °C and 200 °C show tunable electrical properties ($n \sim 10^{16} – 10^{20}$ cm^{-3}) [2]. However, the epitaxial ALD-ZnO layers (thicker than 500 nm) obtained at higher growth temperature (240 °C – 300 °C) exhibit electron concentration at the level of $10^{17} – 10^{18}$ cm^{-3}, which is too high for advanced capacitance spectroscopy-related studies (e.g. DLTS).

In the present work we demonstrate rectifying structures based on the epitaxial ALD-ZnO films and discuss several ways to improve their electrical properties. In particular the effect of Rapid Thermal Annealing (RTA) in the oxygen and nitrogen atmospheres between 300 °C and 500 °C performed on the ZnO samples deposited on Si is shown. This results in a drop of the electron concentration down to $10^{16} – 10^{17}$ cm^{-3}. Interestingly, the Atomic Force Microscopy (AFM) analysis performed prior to and after the annealing steps shows no substantial variation in the RMS roughness as a consequence of the annealing. The layers were subsequently dipped in the 30% solution of H_2O_2 before the Schottky contact (Ag) deposition. The examined ZnO-based structures revealed a rectification ratio of $10^4–10^5$ and an ideality factor η about 2.8 at ± 2V, suggesting their suitability for electrical measurements based on capacitance spectroscopy.

The research was partially supported by the European Union within European Regional Development Fund, through the Innovative Economy grant POIG.01.01.02-00-008/08.
The authors T.A.K., D.S., K.K. and K.G. acknowledge support by the grant number DEC-2013/09/D/ST5/03879 of the National Science Centre of Poland (NCN). The author R.S. was supported by the EU 7th Framework Programme under the CAPACITIES project REGPOT-CT-2013-316014 (EAgLE).

[1] E. Guziewicz, M. Godlewski, T. Krajewski et al., *J. Appl. Phys.* **105**, 122413 (2009).
[2] E. Guziewicz, M. Godlewski, Ł. Wachnicki et al., *Semicond. Sci. Technol.* **27**, 074011 (2012).